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Total power optimization through simultaneously multiple-Vdd multiple-Vth assignment and device sizing with stack forcing

[psu.edu \[PDF\]](#)

W Hung, Y Xie, N Vijaykrishnan, M ... - Proceedings of the ..., 2004 - [ieeexplore.ieee.org](#)  
... and are applied three different operations (reproduction, crossover and mutation) to be a new set of chromosomes – or new **circuit configuration**. ... version of our algorithm (The reason that we cannot achieve a 4X speedup is the interaction overhead among **parallel processes**). ...

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Parallel data processing system using a plurality of processing elements to process data and a plurality of trays connected to some of the processing elements to store ...

H Kato, H Yoshizawa, H Ioku, D Masumoto - US Patent 5,506,998, 1996 - Google Patents  
Page 1. United States Patent Kato et al. US005506998A [ii] Patent Number: [45]  
Date of Patent: 5,506,998 Apr. 9, 1996 [54] PARALLEL DATA PROCESSING SYSTEM  
USING A PLURALITY OF PROCESSING ELEMENTS TO ...

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A system of mixed device-circuit modeling for personal computers

Ni Philatov, DG Yakovlev, BC Nakropin - Solid-State Electronics, 1993 - Elsevier  
... In the case of three element circuit analysis, three **parallel processes** may independently handle the (H, , I, Q, ), (HZ, 02 > Qz)> (H3, ,, Q3) blocks. ... In this case there are some limitations on device complexity and **circuit configuration**. ...

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A programmable I/O system for real-time AC drive control applications

D Woodward, I Page, D Levy, R Harley - Field-Programmable Logic and ..., 1995 - Springer  
... CAD software to layout gate level circuit diagrams or alternatively, Hardware Description Languages (such as VHDL) to define the required **circuit configuration**. ... a single I/O channel (I/O Processor + I/O Port) and thus co-ts of five interconnected **parallel processes** co-operating ...

[Cited by 1](#) - [Related articles](#) - [BL Direct](#) - [All 4 versions](#)

High speed semiconductor memory with burst mode

M Fujita - US Patent 5,835,443, 1998 - Google Patents  
Page 1. United States Patent Fujita US005835443A [ii] Patent Number: 5,835,443  
[45] Date of Patent: Nov. 10, 1998 [54] HIGH SPEED SEMICONDUCTOR MEMORY  
WITH BURST MODE [75] Inventor: Mamoru Fujita, Tokyo ...

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Feedback-free output circuit configuration

G Rumold - US Patent 5,061,571, 1992 - Google Patents  
... 14, 1992 [54] FEEDBACK-FREE OUTPUT **CIRCUIT CONFIGURATION** [75] Inventor: Gerhard Rumold, Bubenreuth, Fed ... send these diagnostic the operation of final controlling elements in industrial ls signals back to the output controller 2 via a **parallel/- processes** and equipment ...

Method for creating parallel processing system

S Hiroshi - US Patent App. 10/562,767, 2004 - Google Patents  
... of elements is stored, hardware configuration information including circuit configurations (a hardware configuration) for executing the **parallel processes** defined by ... the parallel processing system are inputted into the plurality of data inputs of the **circuit configuration** for executing ...

[PDF] Hardware implementation of a digital processing of nuclear medical imaging acquisition and processing system

[wseas.us \[PDF\]](#)

B MAHMOUD, H ESSABBAH, MH BEDOUI - [wseas.us](#)  
... implementation of the different tests of the energy value (E) adherence to a window is achieved in **parallel processes**. ... coefficients, spectrometry windows values, circuit control parameters, **circuit configuration** parameters...) and to calibrate automatically the system in reel time. ...

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Programmable Logic Device and Method for Designing the Same

A Mori, S Manui, M Okamoto - US Patent App. 10/581,024, 2005 - Google Patents  
... **Circuit configuration** information is stored in the configuration memory 202 through the wires 106 through which adjacent logical elements are connected ... process can be distributed and parallelized because it is a process for performing a plurality of **parallel processes** on input ...

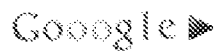
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Semiconductor integrated circuit

T Fukuoka, T Miyazaki, K Tomobe - US Patent App. 10/619,463, 2003 - Google Patents  
... In the VLIW system processor architecture, the hardware is not required to judge possibility of simultaneous execution of each instruction code and the processor can obtain high throughput through the **parallel processes** only by sending, for the purpose of processing, a plurality ...

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